Applicants respectfully assert that the references, taken alone or in combination, fail to teach or suggest each and every feature of the claimed invention as required under §§102(b) 102(e) and 103(a). Applicants further assert that the Office has failed to establish a *prima facie* case of obviousness in support of the §103(a) rejections.

With regard to the rejections of claim 14, Applicants assert that neither Zakel nor Shirai teach or suggest, *inter alia*, first and second substrates including a plurality of partially captured pads, as recited in claim 14. In contrast, Zakel teaches a first substrate 21 having completely uncaptured pads 23 and a second substrate 11 having completely captured pads 24. Although the Office states with regard to Shirai that a first substrate is inherent, Shirai still only teaches using the disclosed method on one substrate.

With regard to the rejections of claims 20 and 24, Applicants assert that neither Shirai nor Lee teach or suggest, *inter alia*, a substrate having a plurality of non-directional conductive pads and a mask thereon, wherein the first dimension of the mask is oriented in the direction of highest stress within interconnections, as recited in claim 20. Likewise, Shirai and Lee fail to teach or suggest, among other things, a mask having a plurality of openings such that the first dimension of the openings coincides with the direction of the highest stress

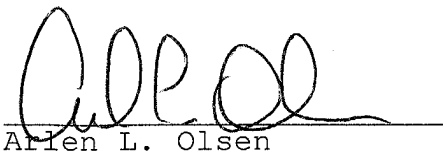
within interconnections formed by the openings, as recited in claim 24.

In contrast, Applicants assert that Shirai teaches nothing about the placement of pads or openings in a direction of highest stress. Furthermore, Shirai teaches directional pads 13, (see Figs. 6-9), wherein orientation is determined by the directional placement of the pads 13, and the direction of the openings 15 in the insulating film 14 are supposed to coincide with the direction of the pads, (see col. 4, lns. 1-9). In other words, it is the direction of pads in Shirai, not the openings in the film, that determine orientation. Likewise, Lee teaches nothing about placing either the pad 100 or the mask opening 210 in a specific direction with regard to highest stress. Moreover, the opening 201 is non-directional, in other words, it is the land 100 that would determine orientation, not the opening as in the present invention.

Applicants respectfully submit that the entire application is in condition for allowance. However, should the Examiner believe anything further is necessary in order to place the application in better condition for allowance, or if the Examiner believes that a telephone interview would be advantageous to

resolve the issues presented, the Examiner is invited to contact the Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,



Arlen L. Olsen
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Date: 4-2-2002

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AMENDED MATERIAL

14. (Amended) An integrated chip package comprising:

a first substrate and a second substrate, wherein [at least one of] the first and second substrates include[s] a plurality of partially captured pads; and

a plurality of interconnections between the first and second substrates.

20. (Amended) A substrate having a plurality of non-directional conductive pads and a mask thereon, wherein the mask has a plurality of openings having a first dimension larger than a diameter of the conductive pad, and a second dimension smaller than the diameter of the conductive pad, and wherein the first dimension is oriented in the direction of highest stress within interconnections formed within the openings of the mask.

23. (Amended) The substrate of claim 22, wherein the first dimension of the openings is selectively oriented in the direction of highest stress within a plurality of interconnections formed within the openings of the [substrate] mask.

24. (Amended) An integrated circuit mask having a plurality of elongated non-circular openings therein, wherein the openings

have a first dimension greater than a second dimension, such that the first dimension of the openings coincides with the direction of the highest stress within [the integrated circuit] interconnections formed by the openings.